Self-Calibrating Memory Controllers

Electronic Design

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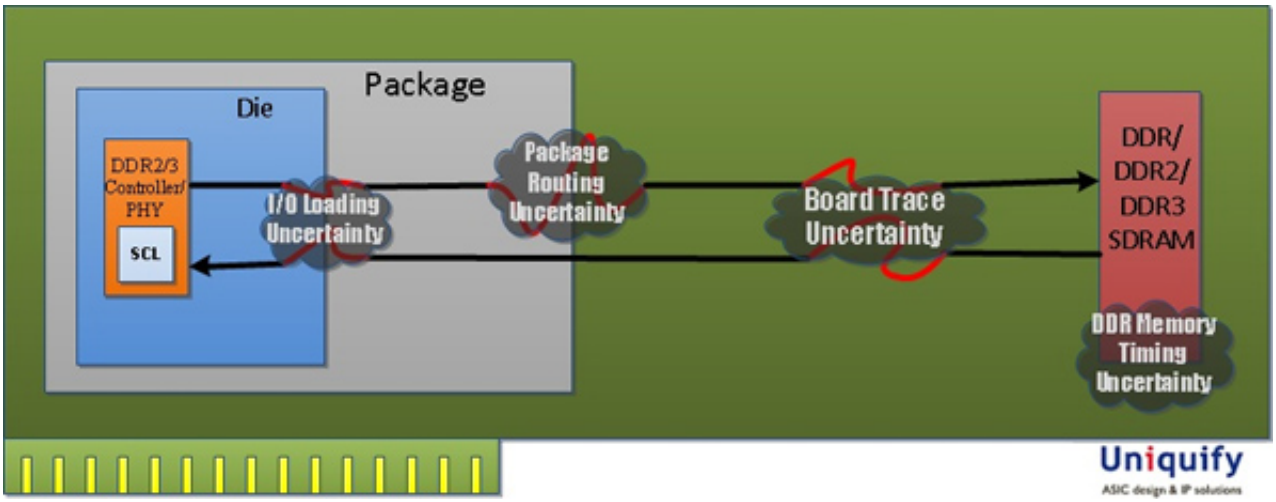
Not all memory controllers are created equally and they are getting harder to build as transistors scale down. I talked with Josh Lee, CEO of Uniquify, about how Uniquify is addressing a major aspect of this challenge.

Uniquify is a Silicon Valley semiconductor IP start-up with a new patent on Self-Calibrating Logic (SCL). SCL can be applied to DDR memory controller designs *(Fig. 1)*. It is designed to automatically fine-tune critical timing parameters.



Wong: What problem does this new "Self Calibrating Logic" Technology Solve?

Lee: Today's deep sub-micron SoC designs integrate DDR memory controllers that operate at multi-GHz clock rates. At these clock rates, system-level memory read-write timing margins are measured in picoseconds. Designing DDR PHYs that satisfy these timing requirements can require exhaustive rounds of incremental IC design modifications, and the resulting silicon often fails to produce high yielding devices in high-volume production.

System level timing requirements are the most challenging part of memory controller design. Precise details about the system board design, the type of external memory devices used, and even details about the host SoC may not be finalized--or may not be well characterized--when the DDR PHY is initially designed.

Wong: How are memory controllers currently designed?

Lee: The conventional approach to managing critical timing requirements is for chip designers to design multiple delay lines into the PHY circuit, and then measure the actual timing characteristics on the first several hundred SoC engineering samples. The optimal clock delay is then manually set using programmable on- chip registers. Permanently setting timing parameters after only a few hundred samples have been fabbed, however, does not always produce high-yielding devices in volume production.

Wong: How does SCL address this problem in a unique way?

Lee: Uniquify's memory controller IP, which incorporates its patented SCL technology, performs a system self-test on power-up that allows the controller's PHY circuitry to automatically select the optimal delay line, fine-tuning the timing parameters every time the host SoC is reset. SCL technology allows Uniquify to move the final determination of exact timing parameters from the IC design stage to system power-on in the field, when all of the characteristics that affect timing are finalized and implemented.

Wong: What advantages does SCL offer chip designers?

Lee: SCL eliminates the need for excessive design tweaks to

achieve timing closure during the SoC development stage. Chips with SCL are much higher yielding due to their ability to automatically adapt their timing characteristics for a wide range of system-level design choices and for variations in the SoC foundry process.

At current process nodes even minor variations in the foundry process can cause timing parameters to drift, which will produce significant yield loss in volume production. SCL automatically accommodates normal process variation--without yield loss--by continuously modifying timing parameters at every power-up. Even system-level aging, which can alter board-level trace delays over years of use, can be accommodated by SCL, thereby improving overall system reliability.

Wong: Is Uniquify's SCL technology actually implemented and in use today?

Lee: Uniquify uses SCL technology in the PHY block of its memory controller IP. The company's DDR1, DDR2, DDR3 and DDR2/3 Combo IPs have been licensed to companies worldwide.

Wong: Can this technology be incorporated into an existing design or do developers need to start from scratch?

Lee: There is NO need to start from scratch. Uniquify incorporates its SCL technology into verified "hard" Memory Controller PHY silicon IP blocks that have been taped-out in multiple foundries and multiple process nodes.

The Memory Controller PHY block is DFI-compliant, so it can be used in conjunction with Uniquify's "soft" DDR2, DDR3 and Combo Memory Controller silicon IP, or integrated with third-party Memory Controller IP. The PHY block that incorporates SCL technology utilizes a minimal subset of the DFI standard, enabling it to be integrated with the widest variety of third-party memory Controller designs. DFI, an industry standard protocol that defines the interface between the PHY and memory controller logic, has been endorsed by recognized leaders in the semiconductor, IP and electronic design automation (EDA) industries, including: ARM, Denali, Intel, LSI Logic, Samsung and ST Microelectronics.

Wong: Is there one optimal configuration or is there a possibility to consider system priorities?

Lee: Based on our interaction with multiple customers and design teams, we have designed SCL technology to maximize both timing margin and performance. By performing the self-calibration test at every power-up, system design choices are automatically accommodated. System board layout, memory

device selection and other system priorities that effect circuit timing are automatically compensated for with SCL technology.

- Uniquify
- DDR PHY Interface

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